76. The stacked gate region of claim 74 wherein said polysilicon structure is at least one ear, said ear being formed adjacent to said field oxide region.

77. A method of fabricating a stacked gate region comprising:

providing a substrate having at least one semiconductor layer;

forming a tunnel oxide layer over said substrate;

forming a first polysilicon layer over said tunnel oxide layer;

forming a nitride layer over said first polysilicon layer;

selectively removing areas of said nitride layer and first polysilicon layer leaving at least one floating gate layer;

patterning trench areas in the substrate;

depositing field oxide in said trench areas;

planarizing a surface of said stacked gate region;

removing said nitride layer;

depositing a second polysilicon layer over said substrate;

selectively removing portions of said second polysilicon layer leaving at least one polysilicon structure adapted to increase capacitive coupling in said stacked gate region.

78. The method of claim 77 further comprising removing a portion of said field oxide.

79. The method of claim 78 wherein said removing said portion of said field oxide is performed before removing said nitride layer.

80. The method of claim 77 wherein said at least one polysilicon structure is selected from the group consisting of at least one single sided ear, and at least one wing.

81. The method of claim 77 wherein said polysilicon structure is at least a pair of single sided

ears, each having one vertical side adjacent to sides of said field oxide and one lower side on one of said at least one floating gate layer.

82. The method of claim 79 wherein said polysilicon structure is at least a pair of wings, each formed adjacent to said at least one floating gate layer and over a portion of said field oxide.

83. A memory cell comprising:

a substrate having at least one semiconductor layer;

a source formed in said substrate;

a drain formed in said substrate;

at least one trench formed in said substrate;

a field oxide region formed in said trench;

a tunnel oxide layer formed over said substrate;

at least one floating gate layer formed over said tunnel oxide layer;

at least one polysilicon structure adapted to increase capacitive coupling of said memory cell;

a dielectric layer formed over said substrate and said floating gate layer; and

a control gate layer formed over said dielectric layer.

84. The memory cell of claim 83 wherein said at least one polysilicon structure is selected from the group consisting of at least one ear, and at least one wing.

85. A method of fabricating a memory cell comprising:

providing a substrate having at least one semiconductor layer;

forming a floating gate layer over said substrate;

forming a trench in said substrate;

forming a field oxide in said trench; and

forming a polysilicon structure adjacent said floating gate layer.

86. The method of claim 85 wherein said polysilicon structure is selected from the group consisting of ears, and wings.

87. A memory device comprising:

a source formed in a substrate;

a drain formed in the substrate;

a floating gate formed over the substrate;

field oxide formed in substrate; and

at least one polysilicon structure formed over the substrate, said polysilicon structure is adapted to increase capacitive coupling of said memory device.

88. The memory device of claim 87 wherein said polysilicon structure is selected from the group consisting of ears, and wings.

89. A computer system comprising:

at least one processor;

a system bus; and

a memory device coupled to said system bus, said memory device including one or more memory cells, each memory cell including at least one stacked gate region comprising:

a substrate having at least one semiconductor layer;

a shallow trench isolation area;

an oxide layer formed over said substrate and said shallow trench isolation area;

a floating gate layer formed over said oxide layer; and

at least one polysilicon structure formed adjacent to said floating gate layer, said at least one polysilicon structure is adapted to increase capacitive coupling of said memory device.